Design Automation of Quantum Circuits for Engineering Systems:

Gate Optimization and Noise-Aware Compilation in NISQ-Aware Hardware

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***Abstract*—The rapid advancement of Noisy Intermediate-Scale Quantum (NISQ) devices has driven the need for efficient design automation tools that can translate complex engineering models into executable quantum circuits. This study explores the development of automated quantum circuit design frameworks focused on gate optimization and noise-aware compilation, enabling practical quantum computation for engineering applications such as optimization, simulation, and control systems. Traditional circuit design methods often fail to account for hardware constraints, decoherence, and gate infidelity, which significantly affect computational accuracy on NISQ devices. To address these challenges, this research introduces a hybrid automation approach combining quantum transpilation, variational circuit pruning, and error-aware synthesis algorithms to enhance circuit reliability and scalability. The framework integrates quantum-classical co-design principles to optimize both logical and physical circuit layers, leveraging hardware-specific calibration data to adapt compilation strategies dynamically. Through simulations and benchmark analysis, the proposed system demonstrates significant improvements in quantum resource utilization, error mitigation, and gate depth reduction compared to conventional compilation methods. This work underscores the growing importance of design automation in quantum engineering, where algorithmic efficiency must be harmonized with physical constraints to realize functional and scalable quantum workflows. By establishing a methodology for gate-level optimization and noise-adaptive design, the study contributes to bridging the gap between theoretical quantum algorithms and real-world engineering implementations within the NISQ computing era.**

The transition from theoretical quantum computation to practical engineering applications requires efficient quantum circuit design automation that can bridge high-level algorithmic models and low-level hardware execution [5]. In the Noisy Intermediate-Scale Quantum (NISQ) era, quantum processors are limited by qubit count, decoherence time, and gate error rates [3]. These hardware imperfections impose severe constraints on circuit depth and fidelity, making noise-aware design and hardware-specific optimization indispensable for achieving reliable computation. Consequently, automated design frameworks that can dynamically adapt to hardware limitations are critical for enabling the deployment of quantum algorithms in engineering contexts such as optimization, energy modeling, process control, and system simulation [4].

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